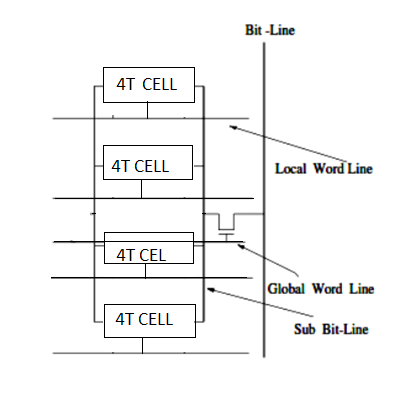
**CHAPTER 5**

**DIVIDED BITLINE TECHNIQUE**

Delay in a memory can be classified into bit line delay and cell delay. Inter connects have capacitance and resistance which contribute to delay. This delay can be less for single cell but in large memories there are a number of rows constituting lengthy bit lines, in turn more bit-line delay. Due to large capacitance and resistance active power consumption also increases.

“Divided bit-line” approach is used for reducing access time and active power consumption by reducing bit-line capacitance. Two or more SRAM cells can be combined together to divide the bit line into several bit lines. These sub bit lines are again connected to a global bit line through a TG or a NFET as shown the in Fig (5.1).



**Fig (5.1) Divided Bit-line approach**

There will be an increase in area about 5-10%, because of precharge and pass transistor for every row and “AND” gate used for each group word-line consisting of M input (M= number of cells in a group) and gate and a NOT gate for a group precharge signal.

**5.1 OPTIMAL GROUPING**

A certain number of cells (M) have to be grouped to get a minmum value of delay,this M is called the optimal value of grouping. to find the optimal value.

Let us consider the following notations.

NFET drain capacitance = Cd

NFET drain resistance = Rd

Capacitance of a unit of Metal 1 = Cm

Resistance of a unit of Metal 1 = Rm

From the tool, metal used for local bitlines is metal 1 and metal used for global bit line is metal 4. Capacitance of metal 4 is half of that of metal 1 and resistance is equal to that of metal 1.

Capacitance of a unit of Metal 4 = Cm/2

Resistance of a unit of Metal 4 = Rm

All the above values are mentioned for a single cell

Toatal number of cells = N

Therfore in a single bitline approach total delay is due to all the drains and metal lines. Total delay can be expressed as

Td = Ct\*Rt

Ct and Rt indicate the total capacitance and resistance at the node.

Ct = N\*(Cd+Cm) (due to N drains and metal interconnects)

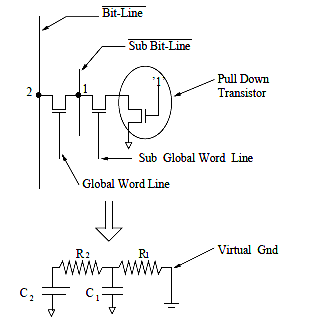
Rt = N\*(Rd+Rm)

Total delay due to single bit line is given by

Td= N\*(Cd+Cm) \*N\*(Rd+Rm) **Eq(5.1)**

Now consider a divided bitline with N rows grouped with M cells each. Here delay is due to global bit line and one sub bitline.

From Fig (5.2) total global bit-line delay (Td2) is due to N metal pieces and N/m drains of pass transistors (N/m because N rows of m bits each will have N/m groups and n/m pass transistors).



**Fig (5.2) RC model**

Therefore Ct = (N\*Cm/2+ (N/M)Cd)

(Cm/2 because metal 4 is used for global bit line)

Rt = [ N\*Cm+ (N/m)\*Cd ]

Now delay Td2 can be written as

Td2 = [ N\*Cm/2+ (N/M)Cd ] \* [ N\*Cm+(N/M)Cd ] **Eq(5.2)**

sub bit line delay (Td1) can be written as sum of delays of (m+2) drains (m drains of access transistor in a m cell group plus one precharge drain one pass transistor drain plus ) and m metal lines which can be written as

Ct = (M+2)Cd +(M+2)Cm

Rt = (M+2)Rd + (M+2)Rm

Td2 = [ (M+2)Cd +(M+2)Cm ]\*[ (M+2)Rd + (M+2)Rm ] **Eq(5.3)**

Now total delay Td can be considered as Td1+Td2

Td = [N\*Cm/2+(N/m)Cd ]\*[ N\*Rm+(N/M)Rd ]

**+** [ ( M+2)Cd +(M+2)Cm ]\*[ (M+2)Rd + (M+2)Rm ] **Eq(5.4)**

From the tool we can observe that Cd=8.5fF Cm=8.5fF and

Rd=40 ohms Rm = 4 ohms

Now we have to find the optimized value of M for which the delay is minimum. We can plot the above equation in MATLAB and find the value of m for minimum value of delay.

**MATLAB results:**



delay

5 10 15 20 25 30

0

No: of cells in a group

**Fig(5.3) Variation of delay with change in grouping**

**5.2 SUMMARY**

In this chapter divided bit line technique is applied on 4T SRAM cells. Delay due to bitline is calculated and equations obtained are plotted in MATLAB to get optimum value of m for which the delay is minimum. As per the MATLAB results optimum value is found to be between 12 and 13, so M=12 is considered and implemented.